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Improvement of resistive switching in NiO-based nanowires by inserting Pt layers

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Nonpolar resistive switching is demonstrated in polycrystalline NiO-based nanowires. The lower switching voltages and narrower switching distributions are exhibited in multilayered NiO/Pt nanowires, compared to the monolithic NiO nanowires. The temperature dependence of resistance at low resistance state reveals the conduction is attributed to the hopping through percolation paths composed of oxygen-related defects. The inserted Pt layers behave as intermediate electrodes to reduce migration length of oxygen ions and to store the oxygen ions near the electrodes. Therefore, the localized formation/migration of oxygen ions confines the occurrence of percolation paths, leading to improvement of the switching parameters. © 2012 American Institute of Physics.

Resistive switching (RS) triggered by the electrical field between the high resistance state (HRS) and the low resistance state (LRS) attracts growing interest for its feasibility to push the advancement of nonvolatile memories toward the next generation due to its structural simplicity and process compatibility with the semiconductor industry.1–3 It has been reported that resistive memory devices based on transition metal oxides, such as NiO,4–7 TiO2,8 or ZnO,9,10 have excellent resistive memory performance.

It is very important to lower the operation electric fields to reduce power consumption and chip size, which are essential for the development of ultra-high density memory technology. Recently, nanowire (NW) memory devices11–18 synthesized by the bottom-up approach19 with the self-assembly mechanism provide an alternative platform to study RS phenomenon at nano-scale. Furthermore, they show great potential for multi-state memory application.12 Unfortunately, the switching voltages of some reported NW-based memory cells are still high12–14 and their distributions are relatively broad,11 which may cause severe problems in controlling and reading memory states. These results are partially due to the fact that the long distance, typically on the order of micrometers, between two electrodes in NW-based devices.20 It is very difficult to make oxide nanowires with the length in the tens of nanometers, typical oxide thickness of RS devices in thin films. Therefore, it becomes quite challenging to obtain narrow distributions of switching voltages in NW-based devices.

It has been reported that oxygen ion or vacancy migration plays a key role on the resistive switching of transition metal oxides.21 The occurrence of the formation/rupture of the percolation paths or conducting filaments near the electrode may suggest the importance of the interfacial reaction between electrode and metal oxide.22,23 Therefore, many efforts have been made to improve the RS characteristics of resistive memory devices through the insertion of an additional layer,5,24–27 or modification of the stoichiometric ratio of oxides,22 to localize the migration of oxygen ions and to reconfigure oxygen-related defects at interface of oxide and electrode.

In this work, we insert Pt layers into monolithic NiO NWs to form a multilayered NiO/Pt NW structure. We investigate the RS behavior in the array of multilayered NiO/Pt NWs, which contain a large number of memory cells with the dimension at tens of nanometers, different from the previous reports in big cells. We demonstrate the nonpolar switching behaviors28,29 in NiO-based NW devices, distinct from the conventional NiO thin film cases. The multilayered NiO/Pt NWs show significantly improved RS characteristics, especially on the low switching voltages and their narrow distributions, which are important factors in realizing the nano-scale memory devices.

Anodic aluminum oxide (AAO) templates with a mean pore diameter of 70 nm were prepared by a two-step anodization process.30 First, high-purity (99.95%) aluminum sheets were anodized under a constant voltage of 40 V in 0.3 M oxalic acid (C2H2O4) solution for 15 min at 1 °C. Afterward, the specimen was immersed in the mixture of 2% chromic acid (CrO3) and 6% phosphoric acid (H3PO4) to remove the top oxide. Then, the second anodization of Al was performed at the same condition as that of 1st anodization but reaction lasted for 6 h. At the end of the second anodization, the voltage was dropped to 0 V at the rate of 0.1 V/s to decrease the thickness of barrier layer at the bottom of the pores. Finally, the pores are widened to 70 nm in 10 wt. % H3PO4 solutions at 30 °C.

The Ni and multilayered Ni/Pt NWs were fabricated in the pores of AAO templates by DC electroplating and cyclic alternative electro-deposition, respectively. The Ni was deposited with reduction potential fixed at −1.3 V versus Ag/AgCl in the sulfate bath containing NiSO4·6H2O (2M),...
were then oxidized at 800°C from 1 to 9 s, while that was fixed at 1 s for Pt. Both samples were then annealed at 800°C for 6 h in air to obtain monolithic NiO and multilayered NiO/Pt NWs. The morphology of NWs embedded into AAO was observed by field emission scanning electron microscopy (FE-SEM) and transmission electron microscopy (TEM). The index of crystallization of the NWs was characterized by x-ray diffractometer (XRD). For electrical measurements, the circle-shaped 60 nm thick Pt top electrode of 200 μm in diameter was deposited on the NW arrays by sputtering with a shadow mask. The aluminum sheet below the AAO template was used as the grounded bottom electrode. RS characteristics of NW devices were investigated by a semiconductor characterization system. The electrical properties were obtained from the NW array to capture the switching behaviors of NWs. Prior to the regular I-V measurements, a forming process was performed at 15 V to initiate RS which changed NiO NWs from the insulating state into the bi-stable reversible state. The compliance current of 0.5 mA was used to protect the device from a permanent breakdown during the SET process, in which the resistance transition from the HRS to the LRS.

The top view FE-SEM image of a polished sample after annealing is shown in the Fig. 1(a), indicating that uniform NWs with the diameter of 70 nm are obtained in AAO with inter-pore distance of 90 nm. Fig. 1(b) shows the x-ray diffraction patterns of monolithic NiO and multilayered NiO/Pt NWs. We can confirm that Ni is completely transformed to NiO and Pt remains metallic after post-oxidation. The TEM images of monolithic NiO and multilayered NiO/Pt NWs with different NiO thicknesses (tNiO) in each segment, shown in Fig. 2, reveal that NWs are polycrystalline structures and clear multilayered structures for Pt insertion, consisting with the results of x-ray diffraction patterns. The tNiO is 50 nm and 100 nm in multilayered NWs shown in Figs. 2(b) and 2(c), respectively. The thickness of Pt and the total length of NWs are fixed at 10 nm and ~6 μm, respectively. Fig. 3(a) shows the typical I-V characteristics of monolithic NiO and multilayered NiO (tNiO = 50 nm)/Pt NW arrays. The SET voltage (VSET) of 6.7 V, at which an abrupt increase in current occurs from HRS (10−7 A) to LRS (10−4 A), is observed for monolithic NiO arrays; the RESET process the resistance transition from the LRS to the HRS, occurs at the voltage (VRESET) of 3.25 V. We observed the coexistence of unipolar and bipolar resistive switching (named as nonpolar switching) in the NiO-based NW devices, that is, the resistive switching behavior is voltage-polarity independent; therefore, we can trigger switching between HRS and LRS by applying either positive or negative electrical field. The ON/OFF ratio of monolithic NiO NW arrays is about 105, which is larger than the reported data in NiO thin film case32 and NW devices.13–15,18 Furthermore, we observe the values of VSET and VRESET are 2.95 V and 1.05 V, respectively, in the multilayered NiO (tNiO = 50 nm)/Pt NW arrays (gray line in Fig. 3(a)), much lower than those of monolithic NiO NW arrays, while the ON/OFF ratio (resistance ratio of HRS to LRS) is kept the same as that of monolithic NiO NW arrays.

To further clarify the dependence of RS characteristics on tNiO, we plot the cumulative probabilities of VSET and VRESET for each sample, as shown in Fig. 4. A wide distribution of switching voltages and relatively large switching voltages are observed for monolithic NiO NW devices. When Pt layers are inserted into NiO NWs to form multilayered structures, lower switching voltages and narrowed distributions are obtained. With reducing tNiO, the average VSET and VRESET as well as the switching voltage distributions are decreased in both unipolar and bipolar operations. As a result, the average operating electrical field of multilayered NWs (~0.5 MV/m) is much lower than thin film cases (~50 MV/m)33 or the

NiCl2 (0.5 M), and H3BO3 (0.5 M). For synthesis of Ni/Pt NWs,31 the electrolytes was modified as the mixture of NiSO4·6H2O (2M), H2PtCl6 (0.002M), and H3BO3 (0.5 M), and the reduction potential was switched between −0.28 V and −1.3 V versus Ag/AgCl to deposit Pt and Ni, respectively. The thickness of Ni was varied by its deposition time with different NiO thicknesses (tNiO) in each segment, shown in Fig. 2, reveal that NWs are polycrystalline structures and clear multilayered structures for Pt insertion, consisting with the results of x-ray diffraction patterns. The tNiO is 50 nm and 100 nm in multilayered NWs shown in Figs. 2(b) and 2(c), respectively. The thickness of Pt and the total length of NWs are fixed at 10 nm and ~6 μm, respectively. Fig. 3(a) shows the typical I-V characteristics of monolithic NiO and multilayered NiO (tNiO = 50 nm)/Pt NW arrays. The SET voltage (VSET) of 6.7 V, at which an abrupt increase in current occurs from HRS (10−7 A) to LRS (10−4 A), is observed for monolithic NiO arrays; the RESET process the resistance transition from the LRS to the HRS, occurs at the voltage (VRESET) of 3.25 V. We observed the coexistence of unipolar and bipolar resistive switching (named as nonpolar switching) in the NiO-based NW devices, that is, the resistive switching behavior is voltage-polarity independent; therefore, we can trigger switching between HRS and LRS by applying either positive or negative electrical field. The ON/OFF ratio of monolithic NiO NW arrays is about 105, which is larger than the reported data in NiO thin film case32 and NW devices.13–15,18 Furthermore, we observe the values of VSET and VRESET are 2.95 V and 1.05 V, respectively, in the multilayered NiO (tNiO = 50 nm)/Pt NW arrays (gray line in Fig. 3(a)), much lower than those of monolithic NiO NW arrays, while the ON/OFF ratio (resistance ratio of HRS to LRS) is kept the same as that of monolithic NiO NW arrays.

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single crystalline NiO NW case (~10 MV/m). Furthermore, the distributions of switching voltages in NiO/Pt multilayered NWs are comparable or even superior to the reported values in NW-based or nanostructure RS cells. Notice that our distributions were obtained from an array of NWs, which contained a large number of cells. Therefore, these statistics should be even better for those measured in a single cell, typically reported in the literature.

To understand the conducting mechanism in NiO-based NWs, we investigated the temperature dependence of resistance at LRS for monolithic NiO NW arrays. As shown in Fig. 3(b), the resistance decreased with increasing temperature, indicating a typical carrier transport behavior in semiconductors. It suggests that conduction in LRS may be attributed to hopping conduction via percolation path composed of oxygen-related defects, which has also been shown in other works as well. Several works reported that the SET process of the RS memory cell is associated with the generation of oxygen vacancies ($V_o$) and the migration of oxygen ions toward the electrode/oxide interface where they are stored, leaving behind the $V_o$ or metal precipitates in the bulk oxide to form percolation paths. The RESET process is associated with the recombination of oxygen ions with the $V_o$. In bipolar RESET process, oxygen ions may migrate from the interface back into the oxide layer and recombine with the $V_o$. In the unipolar RESET process, recombination may occur in the bulk caused by the Joule heating which may induce the oxygen ions from some easily reduced oxide clusters. After the SET process, conduction through hopping can occur through the highly defected structures of NiO NWs so the LRS is achieved; the recombinations of $V_o$ and oxygen ions at the interface and/or bulk during the RESET process lead to low hopping, and thus HRS. Since the recombination can occur either at the interface or in the bulk, the nonpolar RS behavior is observed.

The improved distribution and reduction of switching voltage have been presented in other works by inserting metal layer/crystals, which are ascribed to the region confinement for migration of oxygen ions, leading to localize the formation and annihilation of percolation paths. Because RS in our NiO-based NWs is related to the configuration of oxygen-related defects, the improved switching parameters in multilayered NW arrays may be attributed to the differences of the migration distance of oxygen ions as we change $t_{NiO}$ of NWs. During the SET process, $V_o$ is generated and the oxygen ions migrate toward the anode/oxide interface, where the oxygen ions are accumulated. When defects are increased to a critical number, the percolation paths are formed and hopping occurs easily through percolation paths. Due to the long length between two electrodes in monolithic NiO NW devices, the continuous percolation path from top electrode to bottom electrode may not be easily formed until a larger $V_{SET}$ is applied. The inserted Pt layers behave as intermediate electrodes which increase the probability of connecting locally formed percolation path; therefore, hopping becomes more easily at reduced $V_{SET}$. In addition, oxygen ions are drifted to the anode side by the external bias in the SET process. For multilayered NiO/Pt NW devices, oxygen ions migrate to the intermediate electrodes (Pt), and accumulated near the anode side; therefore, the intermediate Pt electrodes act as the oxygen reservoirs for RS devices. During the RESET process, the oxygen ions can be released from Pt layers to the adjacent NiO layers. The release of oxygen ions can also occur in the bulk for the unipolar operation. The recombination of the $V_o$ and oxygen ions occurs so the percolation paths for hopping are ruptured. The presence of intermediate electrodes (Pt layers) can help the recombination and rupture of the percolation path; therefore, the $V_{RESET}$ is decreased by inserting Pt layers.

By inserting the Pt layers not only the switching voltages are reduced but also the distributions of switching voltages are significantly narrowed (see Fig. 4). The migration length of oxygen ions is quite long between two electrodes in monolithic NiO NW devices so different configurations of oxygen-related defects in each SET/RESET process may exist. Consequently, the hopping may take place along the different locally connected percolation paths for different switching cycles, resulting in wide distributions of $V_{SET}$ and $V_{RESET}$.
$V_{\text{RESET}}$. As the Pt layers are inserted, the confined diameter of NWs and reduced length between adjacent electrodes may significantly localize the formation of the percolation path in each NiO segment. Only limited percolation path can be formed in each NiO segment, resulting in reproducible percolation paths for different switching cycles, and thus narrowed switching distributions. The improved distributions of switching voltages by introducing additional layers in big cells of thin film cases are attributed to the localized electrical fields in the lateral dimension, which leads to the confined percolation paths (or filaments). On the other hand, the percolation paths in the lateral dimension are physically confined in NWs due to the cylindrical geometry at nano-scale. The improvement of the distributions of switching voltages in NiO NWs by inserting Pt layers originates from the confinement of the percolation paths in the reduced NiO thickness. Our findings clearly demonstrate that the distributions of switching voltages can be intrinsically reduced when the cell size approaches the nano-scale due to the physically confined formation of percolation paths.

Our proposed multilayered NW structures can potentially be used in the multi-bit operations. In this work, we use the same materials with the same thickness in each segment. If different materials, for example, CoO and NiO are used for different segments, which can be done by adding one more electrolyte solution and adjusting the reduction voltage during the synthetic process, the multi-bit operation could be achieved with different compliance current or different reset voltages due to different characteristics of various oxides.

In summary, we provide a simple bottom-up approach to fabricate monolithic NiO and multilayered NiO/Pt NWs RS devices, which all showed nonpolar RS behaviors. The significantly improved RS characteristics of lower switching voltages with narrowed distributions were demonstrated in the multilayered NiO/Pt NWs, compared to other monolithic NW devices. We propose that the RS behavior in NiO-based NWs is attributed to the generation and depletion of oxygen defects as well as migration of oxygen ions, leading to the changes of defect states. The migration length of oxygen ions is reduced by inserting Pt layers which act as the oxygen reservoirs during resistance switching. Therefore, the RS characteristics of switching voltages and their distributions can be improved. Our approach and findings can be important for further investigating the RS behaviors at nano-scale.

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